SE2 Power-Aware Signal Processing

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Implementing the vision of ubiquitous multimedia applications for a mobile world will require incorporating power awareness at all levels of portable device design. Power aware digital signal processing (DSP) will form a major component for next-generation portable multimedia platforms such as cellular phones beyond 3G, handheld gaming devices, MP3 players, digital cameras, and mobile television. The Special Evening Topic Session on Power Aware Signal Processing will describe novel circuit, architecture, CAD, and algorithmic techniques for linking system power consumption to signal processing performance, user requirements, and power availability from batteries or energy harvesting from the environment. This session will present papers on a variety of approaches to implement power awareness, including variable precision arithmetic structures, reconfigurable architectures, power optimized libraries, dynamically scalable supply voltages, and variable clocking strategies. These approaches will be described in a variety of application contexts, including wireless sensor nodes, digital still cameras, and portable multimedia devices. The first paper in the session describes an energy scalable computational array which targets mechanical vibration energy harvesting applications. It exploits massive parallelism and the scalability of serial processing to deliver high energy/operation efficiency. The second paper applies mature low power design techniques to reconfigurable architectures with fine-grained control circuitry to implement power awareness for multimedia applications, focusing on video. Digital still camera design is the topic of the third paper, which addresses the challenges to delivering high computation throughput in a limited power budget at all levels of the system hierarchy. The final paper applies task and data-level parallelism to develop image processing techniques which can dramatically lower the power consumption of a smart vision sensor, by trading off communication for local computation. Ultimately, this approach can support ambient intelligence by enabling electronic environments which are aware of and responsive to users.

Position Statements

An Energy Scalable Caomputational Array for Sensor Signal Processing
Rajeevan Amirtharajah, University of California, Davis, CA
Sensor networks have tremendous potential for applications in environmental monitoring, security, and intelligent environments. Scavenging energy can extend sensor mote lifetimes beyond battery limitations, but the available energy is highly variable. Energy scalable approximate processing is a promising technique to maximize DSP performance in this limited-energy context. Additionally, the massive parallelism available from reconfigurable computing fabrics such as FPGAs has been shown to provide higher energy efficiencies than programmable processors for many DSP workloads. However, present commercial FPGA designs offer limited opportunities to enable power-performance tradeoffs. This presentation describes an array of functional units linked by reconfigurable interconnect, currently under development, that implements energy scalability for a number of basic signal processing operations while exploiting the available parallelism. This is achieved through serial processing techniques such as Distributed Arithmetic and an optimized interconnect architecture.

Power Aware Multimedia

Liang-Gee Chen, National Taiwan University, Taipei, Tawan

Reconfigurable hardware architecture is a good design technique for power-aware implementation. It can adjust the power consumption by using mature design techniques, such as operation isolation, clock gating, and voltage scaling, with only a little overhead on area. Besides the area concern, a well-designed reconfigurable architecture can be further combined with a control circuit to realize more fine-granularity power control or content-dependent features. Due to the necessity of cost-performance adaptation in multimedia applications, reconfigurable architectures are very suitable for providing power aware features. In this presentation, the video coding architecture will be used as a design example to demonstrate power adaptation by using reconfigurable system properties. The talk will also highlight the challenges on designing motion estimation, DCT, as well as a video codec for MPEG4 and H.264.

Power Management for Digital Still Camera

Clay Dunsmore, Texas Instruments, Dallas, TX

The digitization of photography has converted chemical complexity (film) into electronic complexity. A mid range consumer digital camera can capture three 8 megapixel images a second. Hundreds of operations are required to process each pixel, resulting in a need for processors that support billions of operations per second. The inclusion of new features such as high definition video encoding is only increasing the computational load. The intent of this presentation is to show that it is possible to provide the required computational throughput while meeting the power requirements of a portable device. Implementing the image preview mode in less than 200 mW will be used as the primary example. Starting at the camera system level and ending up at chip architecture and design, the tradeoffs and techniques used will be presented. These techniques include multiple chip power domains, clock gating, IO power management, power optimized libraries, and voltage scaling.

Wireless Smart Vision for Ambient Intelligence

Richard Kleihorst, Philips Research Laboratories, Eindhoven, The Netherlands

Ambient intelligence is defined as electronic environments that are aware of and responsive to the presence of people. Networks of wireless smart cameras could play a key role for recognising persons, objects and behaviour. Relevant aspects for smart vision are power consumption and image processing performance. Pursuing low power can not be achieved by transmitting video and shifting computation towards a mains powered device because broadcasting raw video data takes up to1 Watt. The ultimate challenge is to do image processing and scene recognition on the ambient sensing device itself and forwarding event descriptions only. We found that task and data-parallelism lowers the power requirements of the smart vision hardware significantly. By matching this with feature-based image recognition algorithms, we are able to cope with complex natural scenes for low power consumption. We will describe the IC design for high-performance low-power imaging and the algorithms that are currently under investigation.